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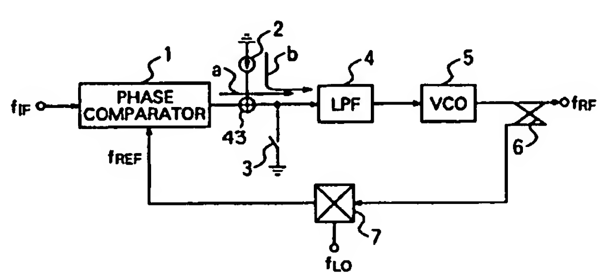
(54) Phase-locked loop circuit and radio communication apparatus using the same

(57) A phase-locked loop circuit includes a current output type phase comparator (1) for converting a phase difference of a first signal (f_{IN}) and a second signal (f_{REF}) into a current signal to be produced, a low pass filter (4) for filtering the current signal of the current output type phase comparator (1) to produce an output signal, a voltage controlled oscillator (5) for producing a signal having a frequency (f_{RF}) corresponding to the output signal of the low pass filter (4) and a frequency converter (7) for frequency-converting the output signal of the voltage controlled oscillator (5) to produce a second signal. A current source (2) is provided for supplying a current which is added to the current signal produced by the phase comparator (1), and the resulting sum current is supplied to an input of the low-pass filter (4). Furthermore a reset switch (3) applies a reset voltage to the voltage controlled oscillator (5) for canceling a phase-locked state of the phase-lock loop circuit.

The phase-locked loop may be used in a transmittor section of a radio communication apparatus, such as a portable terminal of a mobile communication system, to provide for a short frequency settling time and low output noise without broadening of the band of the PLL.

FIG. 1



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Description

BACKGROUND OF THE INVENTION

The present invention relates to a phase-locked loop (hereinafter referred to PLL) for a transmission system included in a portable terminal for converting an intermediate frequency (IF) signal into a radio frequency (RF) signal mainly in the mobile communication and the portable terminal for the radio communication using the PLL.

A PLL system using a local signal frequency f_{LO} to convert an input signal frequency f_{IN} into an output signal frequency f_{LO}-f_{IN} is described in Chapter 10.3 of "PHASELOCK TECHNIQUES" (ISBN0-471-04294-3) issued by John Wiley & Sons and is shown in Fig. 10. In Fig. 10, a phase comparator 18 compares a phase of an input signal frequency f_{IF} with a phase of a reference signal frequency f_{REF} and produces a signal proportional to a phase difference between the two input signals. The output signal of the phase comparator (PD) 18 is supplied to a low pass filter (LPF) 19 in which unnecessary harmonic components and noise are removed from the output signal and an output signal of the low pass filter is supplied to a VCO 20. An output frequency f_{RF} of the VCO 20 is supplied through a coupler 21 to a mixer 22 to be mixed with a local signal frequency f_{LO}. An output frequency f_{REF} of the mixer 22 is given by $f_{REF}=f_{LO}-f_{RF}$. Since the output frequency f_{REF} of the mixer 22 is equal to the frequency f_{IF} when the PLL is in the lock state, the input signal frequency f_{IF} is converted into the output frequency $f_{RF}=f_{LO}-f_{IF}$ of the VCO.

As other examples of the PLL system for the frequency conversion, British Patent No. GB2261345 and United State Patent No. 5313173 may be referred to. These references also use the same method as the fundamental principle of the PLL circuit.

In the above-described circuit, the output signal of the phase comparator is directly supplied to the low pass filter. Accordingly, in order to obtain a shorter settling time, it is necessary to broaden the frequency band of the PLL. On the other hand, however, when the frequency band is broadened, there is a problem that output noise is increased. Further, the circuit described in Chapter 10.3 of "PHASELOCK TECHNIQUES" (ISBN0-471-04294-3) issued by John Wiley & Sons is not considered to be used in a portable terminal.

Fig. 11 illustrates an example of a circuit configuration for shortening the settling time when a voltage output type phase comparator is used. The PLL circuit includes the voltage output type phase comparator 23, a voltage controlled oscillator (VCO) 24, a coupler 25, a mixer 26, a reset switch 27, a power supply 28 for use in shortening of a settling time and a low pass filter 29. Usually, in the PLL circuit, the low pass filter, the VCO and the coupler are mounted on the PLL circuit externally. In this example, since the reset switch 27 and the power supply 28 are connected to the low pass filter 29, the reset switch 27 and the power supply 28 are also mounted on the PLL circuit externally.

While the PLL operation is performed, the reset switch 27 is open (off state). When the PLL circuit is in the phase-locked state, the VCO 24 produces an output signal having a fixed frequency as a center frequency. A small radio communication apparatus such as a portable telephone mostly performs transmission in the time division manner. In this operation, a transmission period in which the PLL circuit is locked to perform transmission with the fixed center frequency and a transmission stop period in which the PLL operation is canceled after the transmission period are performed repeatedly. Further, there is a communication system in which the transmission frequency is changed at a certain period. In such a case, the PLL is locked in the same or different frequency after a predetermined period from cancellation of the locked state. For this end, a voltage for resetting the PLL operation is supplied to the VCO. The reset switch 27 is provided in order to apply the reset voltage. When the reset switch 27 is closed (on state), an input potential of the VCO 24 becomes 0 volt and the output frequency becomes a minimum oscillation frequency.

The voltage output type phase comparator 23 requires an operational amplifier 272 for converting a voltage output into a current output in order to supply a current to a low pass filter 271. The operational amplifier is necessarily required to adjust its operation characteristic and accordingly it is difficult to fabricate the operational amplifier into an IC chip. The negative DC voltage power supply 28 applies a negative bias voltage to an inverted input of the operational amplifier 272 to thereby shorten the settling time of the PLL. Since it is difficult to generate this negative voltage within the IC chip, the circuit of the negative voltage power supply 28 must be disposed outside of the IC chip.

SUMMARY OF THE INVENTION

A phase-locked loop (PLL) circuit according to the present invention employs a phase comparator of current output type. By using the current output type phase comparator in the PLL circuit, it is not required to use an operational amplifier in a low pass filter (LPF). The PLL circuit including the current output type phase comparator, the LPF and a reset switch can be fabricated within an IC chip. Further, when a current source for supplying a current to the LPF is used together with the current output type phase comparator, a time from the start of control of the PLL to the locked state, that is, the settling time can be shortened. The PLL circuit according to the present invention realizes the compatibility of the short settling time or increased settling speed and low output noise without broadening of the band of the PLL.

Furthermore, the radio communication apparatus according to the present invention includes a transmission unit having the PLL circuit using the current output type phase comparator.

In the PLL circuit of the present invention, since an operational amplifier is not required in the LPF and the reset switch is fabricated in an IC chip, reliability and productivity of the PLL can be improved and the radio communication apparatus can be made small.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram illustrating an embodiment of a PLL circuit according to the present invention;
Fig. 2 illustrates a definite embodiment of a low pass filter used in the PLL circuit of the present invention;
Fig. 3 is a diagram showing a definite example of a closed loop transfer function in the embodiment of the PLL circuit of the present invention;
Fig. 4 is a block diagram illustrating another embodiment of a PLL circuit according to the present invention;
Fig. 5 is a block diagram illustrating another embodiment of a PLL circuit according to the present invention;
Fig. 6 is a block diagram illustrating still another embodiment of a PLL circuit according to the present invention;
Fig. 7 is a block diagram illustrating still another embodiment of a PLL circuit according to present invention;
Fig. 8 is a circuit diagram illustrating a definite embodiment of a current output type phase comparator used in the PLL circuit according to the present invention;
Fig. 9 is a circuit diagram illustrating a definite embodiment of a reset switch used in the PLL circuit of the present invention;
Fig. 10 is a block diagram illustrating a general configuration of a PLL circuit;
Fig. 11 is a block diagram illustrating a PLL circuit using a voltage output type phase comparator;
Fig. 12 is a block diagram illustrating an example of a radio communication terminal apparatus using the PLL circuit of the present invention;
Fig. 13 is a block diagram illustrating a PLL circuit of still another embodiment according to the present invention; and
Fig. 14 is a block diagram illustrating a PLL circuit of still another embodiment according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A PLL circuit according to an embodiment of the present invention can be used in a transmitter of a radio communication terminal apparatus such as a portable telephone. Fig. 12 is a block diagram illustrating an example of a radio communication terminal apparatus including the PLL circuit according to the embodiment of the present invention. The communication terminal apparatus can use in various communication systems such as GSM (Global System for Mobile Communications), PDC (Personal Digital Cellular), PCN (Personal Communication Network) and PHS (Personal Handyphone System).

A voice produced by a user is converted into an electric audio signal "Audio in" by means of a microphone (not shown) and is inputted to an input terminal of a transmitter 40.

The audio signal "Audio in" is converted by a digital signal processing processor 30 into I- and Q-channel signals having phases shifted from each other by 90 degrees. The I- and Q-channel signals are then modulated in a modulation mixer 31 and are converted into an IF band frequency. A local oscillation signal is generated by a local signal generator 33 and is phase-shifted by 90 degrees by a 90-degree distributor 32 to be supplied to the modulation mixer 31. Thereafter, the signal produced by the mixer 31 is converted by a PLL circuit 34 of the present invention into a frequency of a transmission frequency band. A local oscillation signal supplied to the PLL circuit 34 is generated by a local signal generator 35. An output signal of the PLL circuit 34 is amplified by an output amplifier 36 and then transmitted from an antenna 38 through a switch 37, which is connected to the antenna 38, the transmitter including the processor 30, the mixer 31, the distributor 32, the local signal oscillator 33, the PLL 34, the local signal oscillator 35 and the amplifier 36 and a receiver 39.

The circuit portion including the mixer 31, the 90-degree distributor 32, the PLL 34 and a part of the receiver 39 in an area surrounded by broken line of Fig. 12 can be fabricated in a single IC chip.

Referring now to Figs. 1 to 9, the structure and operation of the PLL circuit according to the embodiment of the present invention are described.

Fig. 1 illustrates a basic configuration of a PLL circuit according to the embodiment of the present invention. The PLL circuit includes a current output type phase comparator 1, a constant current source 2, a reset switch 3, a low pass filter 4, a VCO 5, a coupler 6 and a mixer 7. The constant current source 2 supplies a constant current (shown by arrow b) from the ground toward an input terminal of the low pass filter 4. The reset switch 3 is connected between the input terminal of the low pass filter 4 and the ground. The reset switch 3 is open during operation of the PLL circuit.

The current output type phase comparator 1 compares a phase of an input signal frequency f_{IF} with a phase of a reference signal frequency f_{REF} and produces a current proportional to a phase difference thereof. When the PLL circuit is operated, the reset switch 3 is open. In order to shorten the settling time of the PLL, the output current (shown by arrow a) of the phase comparator 1 is added to the constant current (shown by arrow b) produced from the constant current source 2 in an adder 43 and a sum current thereof is

supplied to the low pass filter 4. Incidentally, the adder 43 is merely signal lines combined with each other. When the current output type phase comparator 1 is operated by itself and the phase difference of the two input signals f_{IF} and f_{REF} is varied, the condition for causing the PLL to perform the stable settling operation is obtained experimentally and is given by the following equation (1):

$$\frac{0.5\,(I_{MAX} - |I_{MIN}| + I_{OFF}}{I_{MAX}} \leq 0.6 \qquad (1)$$

where the maximum value and the minimum value of the DC component of the output current are I_{MAX} and I_{MIN}, respectively, and the output current of the constant current source 2 is I_{OFF}.

The low pass filter 4 removes unnecessary harmonic components and noise from the sum current of the outputs of the current output type phase comparator 1 and the constant current source 2 and converts the sum current into a voltage signal to be supplied to the VCO 5. The output frequency f_{RF} of the VCO 5 is inputted through the coupler 6 to the mixer 7 to be mixed with the local oscillation signal frequency f_{LO}. The output frequency f_{REF} of the mixer 7 is given by $f_{REF}=f_{LO}-f_{RF}$. When the PLL is in the locked state, the output frequency f_{REF} of the mixer 7 is equal to f_{IF}. Accordingly, the input signal frequency f_{IF} is converted into $f_{RF}=f_{LO}-f_{IF}$.

Fig. 2 illustrates a definite circuit of an embodiment of the low pass filter 4. Electric charges are stored in the low pass filter 4 by a DC component of the output current of the current output type phase comparator 1. A charged voltage is supplied to the VCO 5 as the output voltage of the low pass filter 4. At the same time, electric charges are also stored in capacitors C_1 and C_2 of the low pass filter 4 by the constant current produced from the constant current source 2 and accordingly the speed of storing the electric charges is increased as compared with the case where the constant current source 2 is not provided. Consequently, the settling time of the PLL is shortened.

The current supplied from constant current source 2 to the low pass filter 4 may be controlled to be a predetermined constant current from the beginning or a considerable large current temporarily at the beginning and a slightly small constant current thereafter. In the latter case, the speed of storing the electric charges can be increased as compared with the former case.

The transfer function F(s) of the low pass filter 4 is given by the following equation (2):

$$F(s) = \frac{s + \dfrac{1}{C_2R_1}}{C_1s(S + \dfrac{C_1 + C_2}{C_1C_2R_1})} \qquad (2)$$

Operation of the PLL circuit is analyzed when the filter circuit shown in Fig. 2 is used as the low pass filter 4 of Fig. 1. When the phase difference conversion gain of the current output type phase comparator 1 is K_d [A/rad] and the sensitivity of the VCO 5 is K_v [rad/s/V], the open loop transfer function Ho(s) of the PLL is given by the following equation (3):

$$Ho = K_dF(s)\frac{K_v}{s} \qquad (3)$$

$$= \frac{K_dK_v(s + \dfrac{1}{C_2R_1})}{C_1s^2(s + \dfrac{C_1 + C_2}{C_1C_2R_1})}$$

At this time, a pole ω_z [rad/s] and a zero ω_p [rad/s] of the PLL are given by the following equations (4) and (5), respectively:

$$\omega_z = \frac{1}{C_2R_1} \qquad (4)$$

$$\omega_p = \frac{C_1 + C_2}{C_1C_2R_1} \qquad (5)$$

Fig. 3 shows an example of a frequency characteristic of a closed loop transfer function Hc(s) of the PLL. As shown in Fig. 3, the loop shows the characteristic of the low pass filter. Accordingly, the frequency modulation and the phase modulation within the loop band can be reproduced at the output of the VCO and unnecessary signals beyond the band can be suppressed. However, when the loop band is made too narrow, the modulation accuracy at the output of the PLL is deteriorated and when the loop band is made too broad, it is insufficient to suppress noise beyond the band. In order to satisfy the standard such as GSM, it is necessary to select the loop band from the range of 1 MHz to 3 MHz.

Fig. 4 illustrates a PLL circuit according to another embodiment of the present invention. The PLL circuit includes a current output type phase comparator 1, a constant current source 2, a reset switch 3, a low pass filter 4, a VCO 5, a coupler 6, a mixer 7 and a power supply 8. The constant current source 2 produces a constant current (shown by arrow b) flowing from an input terminal of the low pass filter 4 to the ground. The reset switch 3 is connected between the input terminal of the low pass filter 4 and the power supply 8.

The current output type phase comparator 1 compares a phase of an input signal frequency f_{IF} with a phase of a reference signal frequency f_{REF} and produces a current proportional to a phase difference thereof. When the PLL circuit is operated, the reset switch 3 is open. In order to shorten the settling time of

the PLL circuit, the constant current (arrow b) produced from the constant current source 2 is added to an output current (arrow a) of the current output type phase comparator 1 and a sum current thereof is supplied to the low pass filter 4.

Operation of the PLL circuit of Fig. 4 in which the low pass filter 4 shown in Fig. 2 is used is now described. When the reset switch 3 is closed to perform the reset operation, the capacitors C_1 and C_2 of the low pass filter 4 are charged by a positive voltage of the power supply 8. The voltage of the power supply 8 is set to a value higher than an input voltage of the VCO 5 at the time when the PLL circuit has completed the settling operation (upon the locked state). When the reset switch 3 is opened and the PLL operation is started, the electric charges stored in the capacitors C_1 and C_2 are discharged toward the constant current source 2 and the phase comparator 1. The constant current source 2 facilitates the discharge of positive electric charges from the capacitors C_1 and C_2. Consequently, the settling time of the PLL circuit is shortened.

When the current output type phase comparator 1 is operated by itself and the phase difference of the two input signals is varied, the condition for causing the PLL to perform the stable settling operation is obtained experimentally and is given by the following equation (6):

$$\frac{0.5(|I_{MIN}| - I_{MAX}) + I_{OFF}}{|I_{MIN}|} \leq 0.6 \qquad (6)$$

where the maximum value and the minimum value of the DC component of the output current are I_{MAX} and I_{MIN}, respectively, and the output current of the constant current source 2 flowing from the input terminal of the low pass filter 4 to the ground is I_{OFF}.

The low pass filter 4 removes unnecessary harmonic components and noise from the sum current of the outputs of the current output type phase comparator 1 and the constant current source 2 and converts the sum current into a voltage signal to be supplied to the VCO 5. The output frequency f_{RF} of the VCO 5 is inputted through the coupler 6 to the mixer 7 to be mixed with the local oscillation signal frequency f_{LO}. The output frequency f_{REF} of the mixer 7 is given by $f_{REF}=f_{LO}-f_{RF}$. When the PLL is in the locked state, the output frequency f_{REF} of the mixer 7 is equal to f_{IF}. Accordingly, the input signal frequency f_{IF} is converted into $f_{RF}=f_{LO}-f_{IF}$.

Fig. 5 illustrates another embodiment of the present invention. The PLL circuit of Fig. 5 is characterized in that limiters 9 and 10 are connected to the input portions of the current output type phase comparator 1 in the same configuration of the PLL circuit of Fig. 1. When a mixer type circuit using bipolar transistors is employed in the current output type phase comparator 1 and an amplitude of an input signal is smaller than kT/q where q is an amount of electric charges of electrons, k is a Boltzmann's constant, and T is an absolute temperature, the phase difference conversion gain of the current output type phase comparator 1 has the dependency on the input amplitude. The limiters 9 and 10 amplify the input signals to the current output type phase comparator 1 to increase the amplitude of the input signal f_{RF} to a constant amplitude larger than kT/q, so that the phase difference conversion gain of the phase comparator 1 can be made constant.

Fig. 6 illustrates another embodiment of the present invention. The PLL circuit of Fig. 6 is characterized in that low pass filters 11, 12, 13 and 14 are connected in the same configuration as the PLL circuit of Fig. 5. The low pass filters 13 and 14 are used to prevent unnecessary harmonics from being inputted to the limiters 9 and 10. Since the limiters 9 and 10 produce the signals having the constant amplitude, the output signals of the limiters 9 and 10 contain unnecessary harmonic components. Accordingly, the low pass filters 11 and 12 removes the unnecessary harmonic components.

Fig. 7 illustrates another embodiment of a PLL circuit according to the present invention. The PLL circuit of Fig. 7 is characterized in that an amplifier 15 is connected between the coupler 6 and the mixer 7 in the same configuration as the PLL circuit of Fig. 1. By connecting the amplifier 15, the PLL circuit can be operated even when the output of the VCO has a small amplitude.

Fig. 8 illustrates an embodiment of the current output type phase comparator 1. Transistors may be of bipolar type. VDD is a power supply voltage. Numeral 16 denotes a so-called Gilbert multiplier. Detail thereof is described in Chapter 10.3 of "DESIGN TECHNIQUE OF ANALOG INTEGRATED CIRCUIT FOR SUPER LSI (Last Volume)" issued by Baifukan. The Gilbert multiplier 16 mixes input signals V_{IF}^+ and V_{IF}^- and reference signals V_{REF}^+ and V_{REF}^- to produce differential currents I_4 and I_5 having phases opposite to each other. Bases of transistors Q2 and Q3 are applied with the signal V_{REF}^- having the phase opposite to that of the signal applied to bases of transistors Q1 and Q4. Similarly, a base of transistor Q6 is applied with the signal V_{IF}^- having the phase opposite to that of the signal applied to a base of a transistors Q5. When amplitudes of the input signals V_{IF}^+ and V_{IF}^- and the reference signals V_{REF}^+ and V_{REF}^- are larger than kT/q and a collector current of a transistor Q11 is I_6, the relation of a phase difference ϕ of the input signals V_{IF}^+ and V_{IF}^- and the reference signals V_{REF}^+ and V_{REF}^- and a differential current I_4-I_5 produced by the Gilbert multiplier 16 is given by the following equation (7):

$$I_4 - I_5 = I_6\left(\frac{2\phi}{\pi}-1\right) \qquad (7)$$

Transistors Q11, Q12 and Q13, resistors R6 and R7 and a constant current source I_{REF} constitute a bias cir-

cuit of the Gilbert multiplier 16 using the current mirror circuit. The transistor Q11 constitutes a current source for the transistors Q5 and Q6 connected to the collector of the transistor Q11.

Numeral 17 denotes a charge pump circuit which converts the output differential currents I_4 and I_5 of the Gilbert multiplier 16 into a single-ended output signal to produce it as a current I_{out}. Transistors Q7 and Q8 and resistors R1 and R3 constitute a current mirror circuit. When a current mirror ratio determined by characteristics of the resistors R1 and R3 and the transistors Q7 and Q8 is a, the relation of $I_3=a \cdot I_4$ is obtained. Similarly, transistors Q9 and Q10 and resistors R2 and R4 constitute a current mirror circuit. When a current mirror ratio thereof is b, the relation of $I_1=b \cdot I_5$ is obtained. Further, transistors Q14, Q15 and Q16 and resistors R8 and R9 also constitute a current mirror circuit. When a current mirror ratio thereof is c, the relation of $I_2=c \cdot I_3$ is obtained. The currents I_1 and I_2 are used to obtain $I_{OUT}=I_1-I_2$.

Fig. 9 illustrates an embodiment of the reset switch. That is, the reset switch corresponds to the reset switch 3 of Fig. 1. Transistors of bipolar type are used.

VDD is a power supply voltage. A constant current source I_E is a bias circuit for the reset switch 3 and supplies a bias current to transistors Q17 and Q18. Transistors Q19 and Q20 and resistors R11 and R12 constitute a current mirror circuit and when a current mirror ratio thereof is d, the relation of $I_8=d \cdot I_7$ is obtained. When a voltage applied to an input terminal IN for control of the time division operation is larger than the reference voltage V_{REF}, a transistor Q18 is turned off, so that currents I_7 and I_8 scarcely flow and transistors Q19 and Q20 are also turned off. When a base current of the transistor Q21 is neglected since the base current is small, a base voltage of a transistor Q21 is given by $R10 \cdot I_8$, while since the current I_8 scarcely flows, the transistor Q21 is turned off, so that a collector current of the transistor Q21 hardly flows. Accordingly, the reset switch 3 becomes the off (open) state. When the voltage applied to the input terminal is smaller than the reference voltage V_{REF}, the transistor Q18 is turned on and the current I_8 is $I_8=d \cdot I_7 \sim d \cdot I_E$. Accordingly, the base voltage of the transistor Q21 is substantially equal to $R10 \cdot d \cdot I_E$. When the current I_E is set so that the transistor Q21 is turned on when the base voltage is equal to $R10 \cdot d \cdot I_E$, the transistor Q21 is turned on, so that a terminal OUT is connected to the ground and the reset switch 3 becomes the on (close) state.

The circuits shown in Figs. 8 and 9 employ bipolar transistors, while transistors of other kinds such as, for example, MOSFET and MESFET may be used to realize the same function.

Fig. 13 illustrates a PLL circuit according to another embodiment of the present invention. The PLL circuit of Fig. 13 is characterized in that a frequency divider 41 is connected between the current output type phase comparator 1 and the coupler 6 instead of the mixer 7 in the same configuration as the PLL circuit of Fig. 1. A frequency division ratio of the frequency divider 41 is given by f_{RF}/f_{IF}.

Fig. 14 illustrates a PLL circuit according to still another embodiment of the present invention. The PLL circuit includes a current output type phase frequency comparator 42, a low pass filter 4, a VCO 5, a coupler 6 and a mixer 26. When the phase difference between the input signal f_{IF} and the reference signal frequency f_{REF} is small, the current output type phase frequency comparator 42 compares a phase of the input signal f_{IF} with a phase of the reference signal frequency f_{REF} and produces an error output current. When the phase difference between the input signal f_{IF} and the reference signal frequency f_{REF} is not small, the current output type phase frequency comparator 42 compares a frequency of the input signal f_{IF} with a frequency of the reference signal frequency f_{REF} and produces an error output current. The low pass filter 4 removes unnecessary harmonic components and noise from the output current of the comparator 42 and converts the output current into a voltage to be supplied to the VCO 5. An output frequency f_{RF} of the VCO 5 is inputted to the mixer 26 through the coupler 6 and is mixed with the local oscillation signal frequency f_{LO} in the mixer 26. An output frequency f_{REF} of the mixer 26 is equal to f_{IF} when the PLL circuit is in the locked state. Accordingly, the input signal frequency f_{IF} is converted into $f_{RF}=f_{LO}-f_{IF}$.

The phase comparator is named a phase frequency comparator (PFC). Since the PLL circuit is necessarily locked without the provision of a switch when the PFC is used, the reset switch is not required. However, since the output voltage of the phase comparator is not once reduced to 0 volt by means of the reset switch, the PLL circuit may be operated even if the constant current source for increasing the settling speed is provided, while the settling time is not necessarily shortened.

As described above, according to the present invention, since the phase comparator produces the current output and the constant current is further added to the current output, the setting time can be shortened without widening of the band for the PLL circuit. Furthermore, since the settling time shortening circuit and the reset switch are connected to the phase comparator, the circuit configuration suitable for the integrated circuit can be realized.

Claims

1. A phase-locked loop circuit comprising:

    a current output type phase comparator (1) for converting a phase difference between a first signal (f_{IN}) and a second signal (f_{REF}) into a current signal to be outputted;
    a low pass filter (4) for filtering said current signal of said current output type phase compara-

tor (1) to produce an output signal;

a voltage controlled oscillator (5) for producing a signal having a frequency (f_{RF}) corresponding to said output signal of said low pass filter (4); and

a frequency converter (7) for frequency-converting an output signal of said voltage controlled oscillator (5) to produce said second signal.

2. A phase-locked loop circuit according to Claim 1, further comprising a current source (2) for supplying a current to an input of said low pass filter (4).

3. A phase-locked loop circuit according to Claim 2, further comprising a reset switch (3) for applying to said voltage controlled oscillator (5) a reset voltage for canceling a phase-locked state of the phase-locked loop.

4. A phase-locked loop circuit according to Claim 3, further comprising a coupler (6) for distributing said output signal of said voltage controlled oscillator (5) into an output terminal of said phase-locked loop circuit and an input of said frequency converter (7).

5. A phase-locked loop circuit according to Claim 4, wherein said low pass filter (4) includes capacitors (C1, C2) for shunting a predetermined frequency component of an input signal thereto and which are supplied with electric charges by said current source (2).

6. A phase-locked loop circuit according to Claim 5, wherein said current source includes a constant current source (2) for supplying a constant current to the input of said low pass filter (4) and for supplying electric charges to said capacitances.

7. A phase-locked loop circuit according to Claim 5, further comprising a DC voltage source (8) connected to said reset switch (3) for generating said reset voltage, which is higher than an input voltage of said voltage controlled oscillator (5) when the phase-locked loop is in the phase-locked loop, and wherein said current source includes a constant current source (2) for supplying a constant current so that the current is pulled out from the input of said low pass filter (4) when said reset switch is not operated.

8. A phase-locked loop circuit according to Claim 1, wherein said frequency converter includes a mixer circuit (7) having two inputs, one of which is supplied with the output signal (f_{RF}) of said voltage controlled oscillator (5) and the other of which is supplied with a signal having a predetermined frequency (f_{LO}), and for generating an output signal (f_{REF}) in accordance with a difference frequency of said two input signals to be supplied to said current output type phase comparator (1) as said second signal.

9. A phase-locked loop circuit according to Claim 1, wherein said frequency converter includes a frequency divider (41) for frequency-converting the output signal of said voltage controlled oscillator (5) to produce said second signal.

10. A phase-locked loop circuit according to Claim 6, wherein when said current output type phase comparator (1) is operated by itself and a phase difference between said two input signals is varied, said current output type phase comparator satisfies the following equation:

$$(0.5(I_{MAX}-|I_{MIN}|)+I_{OFF})/I_{MAX} \leq 0.6$$

where I_{MAX} and I_{MIN} are maximum and minimum values of a DC component of the output current, respectively, and I_{OFF} is a value of an output current of said constant current source flowing toward the input of said low pass filter.

11. A phase-locked loop circuit according to Claim 7, wherein when said current output type phase comparator (1) is operated by itself and a phase difference between said two input signals is varied, said current output type phase comparator satisfies the following equation:

$$(0.5(|I_{MIN}|-I_{MAX})+I_{OFF})/|I_{MIN}| \leq 0.6$$

where I_{MAX} and I_{MIN} are maximum and minimum values of a DC component of the output current, respectively, and I_{OFF} is a value of an output current of said constant current source flowing out from the input terminal of said low pass filter.

12. A phase-locked loop circuit according to any one of Claims 1 to 11, further comprising a first limiter (10) for limiting an input signal to said first signal having a fixed amplitude to be outputted and a second limiter (9) for limiting the output signal of said frequency converter (7) to said second signal having a fixed amplitude.

13. A phase-locked loop circuit according to Claim 12, further comprising a second low pass filter (14) for filtering the input signal of said phase-locked loop circuit to produce an output signal and supplying said output signal to said first limiter (10), a third low pass filter (11) for filtering an output signal of said first limiter to produce said first signal and supplying said first signal to said current output type phase comparator (1), a fourth low pass filter (13) for filtering the output signal of said frequency converter (7)

to produce an output signal and supplying said output signal to said second limiter (9), and a fifth low pass filter (12) for filtering an output signal of said second limiter to produce said second signal and supplying said second signal to said current output type phase comparator (1).

14. A phase-locked loop circuit according to any one of Claims 1 to 11, further comprising an amplifier (15) for amplifying an output signal of said voltage controlled oscillator (5) to supply it to said frequency converter (7).

15. A phase-locked loop circuit according to Claim 2 or 3, wherein said current output type phase comparator includes a Gilbert multiplier (16) and first, second and third current mirror circuits, and said first and second input signals are supplied to differential inputs of said Gilbert multiplier, third and fourth signals which are differential output currents of said Gilbert multiplier being supplied to said first and second current mirror circuits, respectively, an output current of said second current mirror circuit being supplied to said third current mirror circuit, output currents of said third and first current mirror circuits being added to constitute the output current of said current output type phase comparator.

16. A phase-locked loop circuit according to Claim 1, 12, 13 or 14, wherein a loop band width of said phase-locked loop circuit is between 1 MHz to 3 MHz. 17. A radio communication apparatus including a transmitter (40), a receiver (3), an antenna (38), and a duplexer (37) for selectively coupling any of an input of said receiver and an output of said transmitter to said antenna, wherein said transmitter (40) comprises:

said phase-locked loop circuit set forth in any of Claims 1 to 16 for converting a frequency of the input signal to a transmission frequency to supply it to said voltage controlled oscillator (5); and
an output amplifier (36) for amplifying an output signal of said voltage controlled oscillator (5) to produce an output signal of said transmitter.

FIG. 1

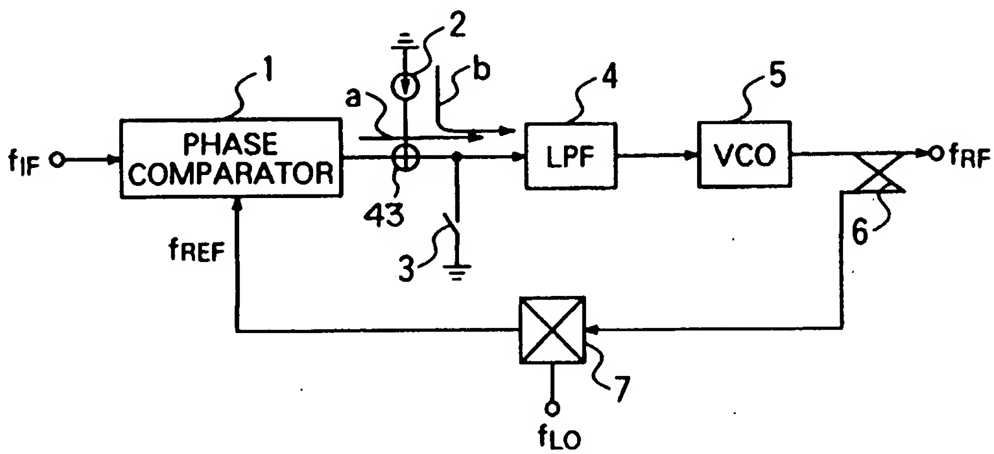

2
b
1
a
4
5
fIF
PHASE COMPARATOR
LPF
VCO
fRF
43
6
fREF
3
7
fLO

FIG. 2

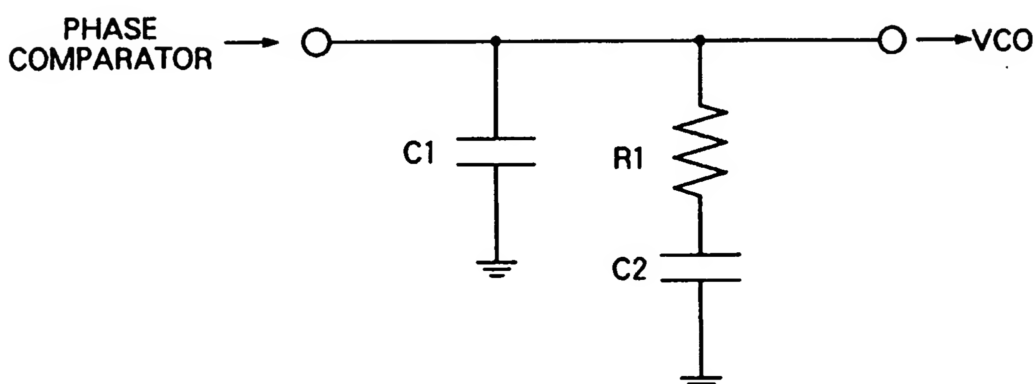

PHASE COMPARATOR
VCO
C1
R1
C2

FIG. 3

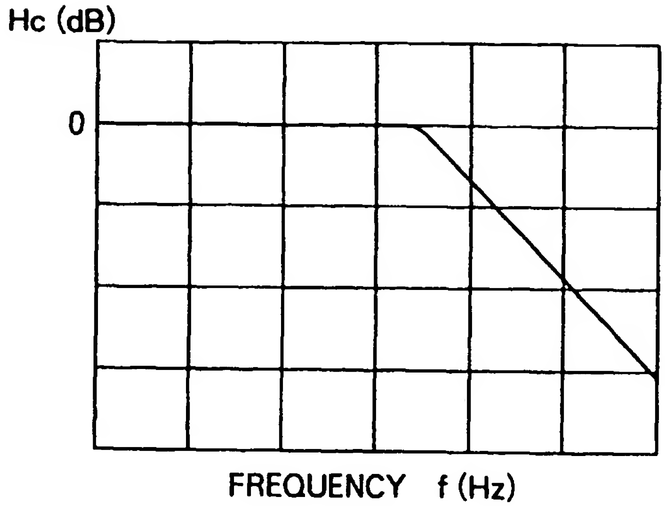

Hc (dB)
0
FREQUENCY f (Hz)

FIG. 4

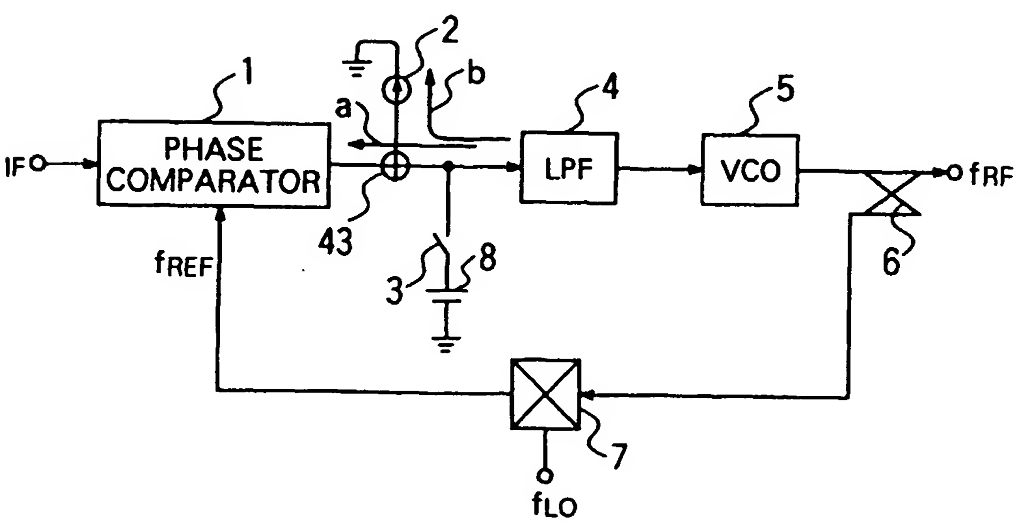

1
2
b
a
4
5
IF
PHASE COMPARATOR
LPF
VCO
fRF
43
fREF
3
8
6
7
fLO

FIG. 5

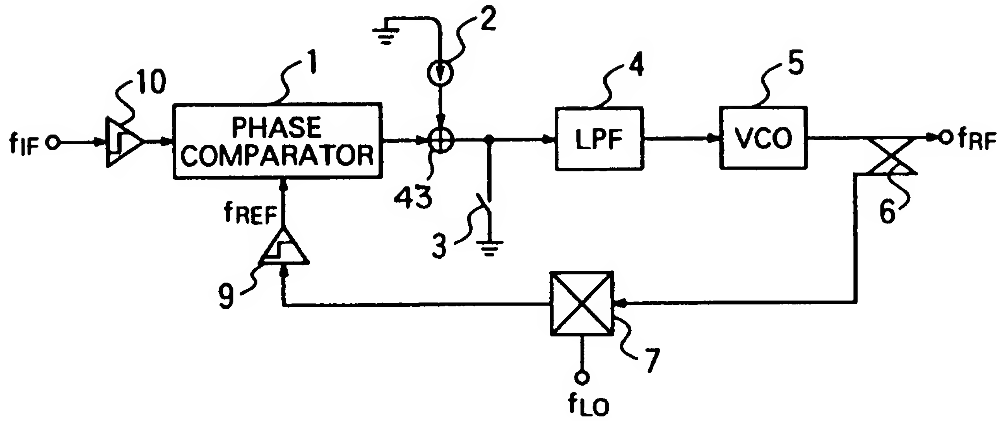

2
1
10
4
5
PHASE COMPARATOR
LPF
VCO
fIF
fRF
43
fREF
3
6
9
7
fLO

FIG. 6

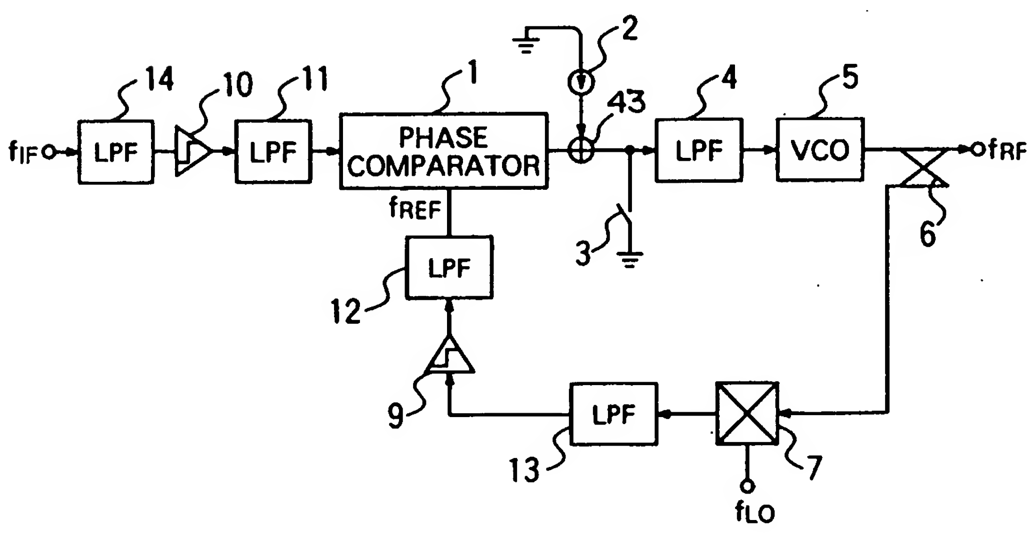

2
14
10
11
1
43
4
5
fIF
LPF
LPF
PHASE COMPARATOR
LPF
VCO
fRF
fREF
LPF
6
3
12
9
LPF
13
7
fLO

FIG. 7

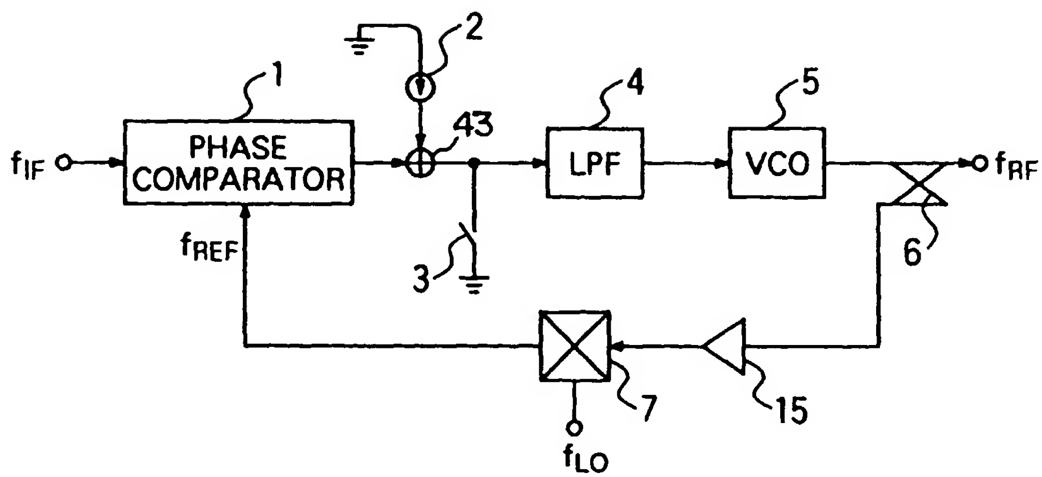


FIG. 8

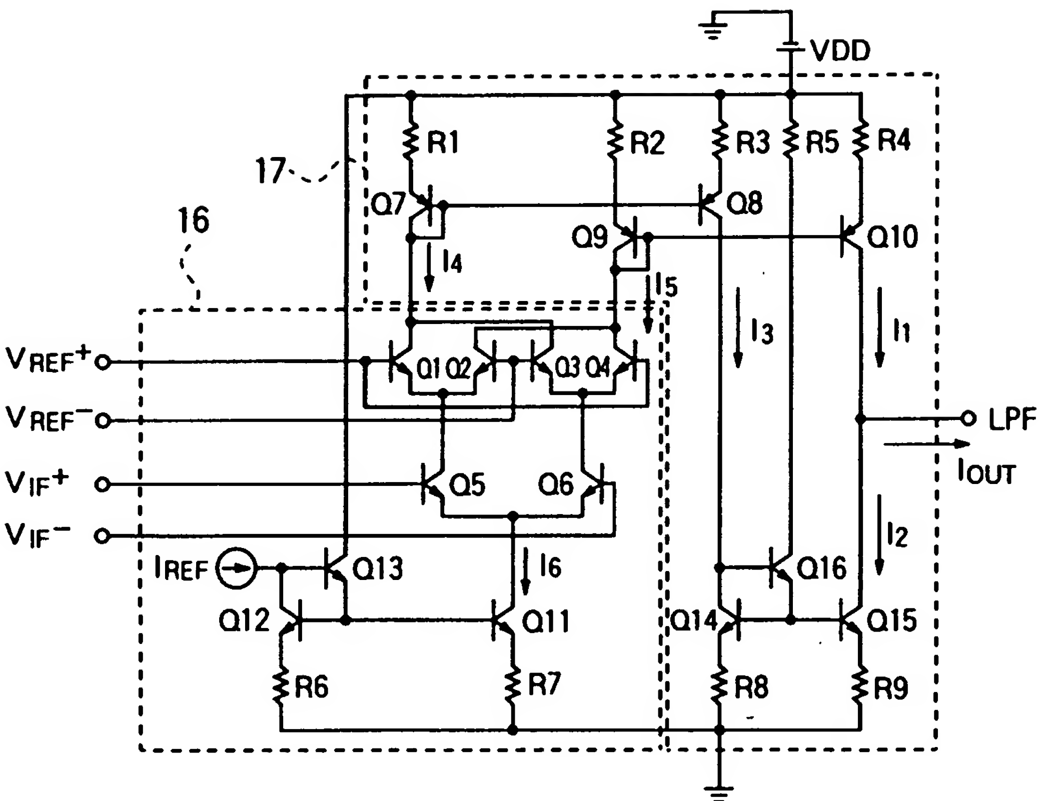

VDD
R1
R2
R3
R5
R4
17
16
Q7
Q8
Q9
Q10
I4
I5
I3
I1
VREF+
VREF−
VIF+
VIF−
Q1 Q2
Q3 Q4
Q5
Q6
LPF
IOUT
I2
IREF
Q13
I6
Q16
Q12
Q11
Q14
Q15
R6
R7
R8
R9

FIG. 9

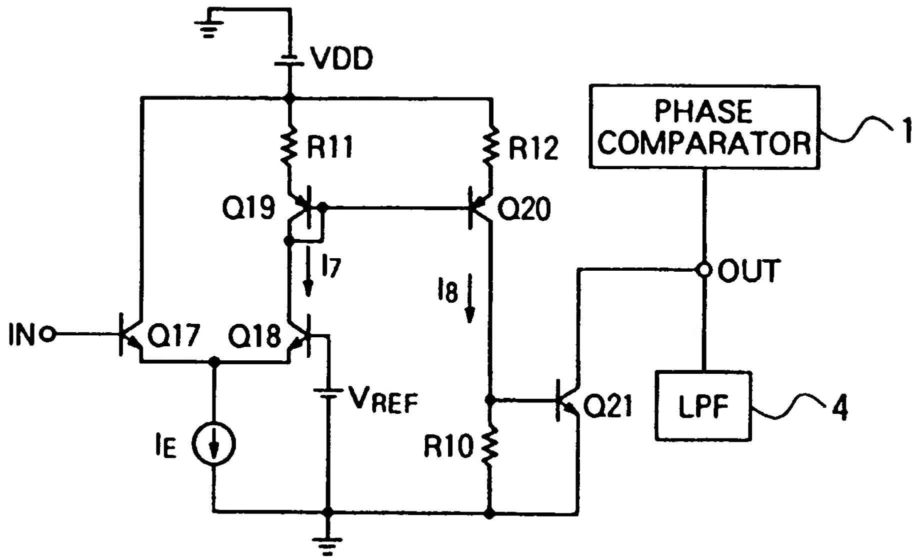

VDD
R11
R12
PHASE COMPARATOR
1
Q19
Q20
I7
I8
OUT
IN
Q17
Q18
VREF
Q21
LPF
4
IE
R10

FIG. 10

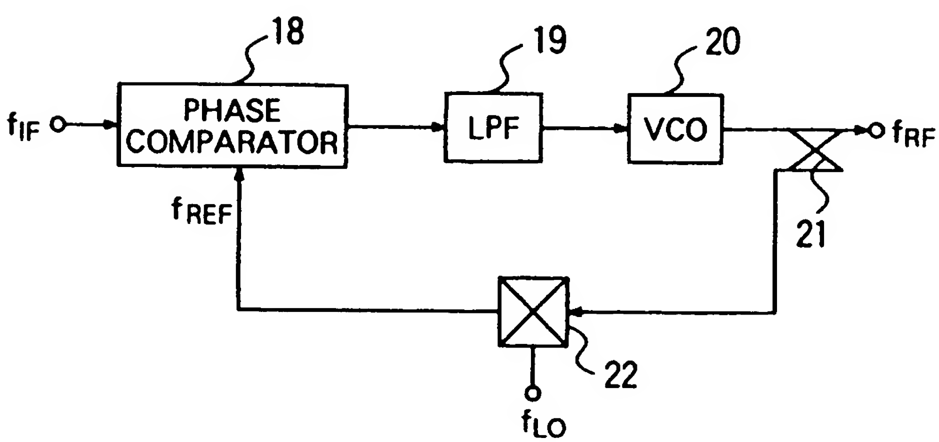

18
19
20
fIF
PHASE COMPARATOR
LPF
VCO
fRF
fREF
21
22
fLO

FIG. 11

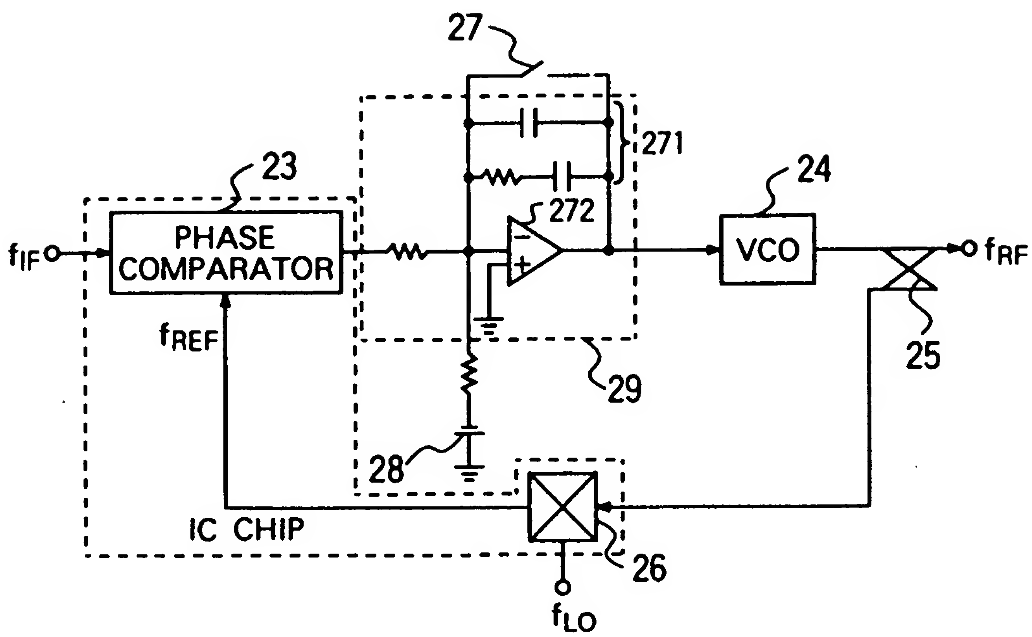

27
271
23
24
272
PHASE
COMPARATOR
VCO
f_{IF}
f_{RF}
f_{REF}
25
29
28
IC CHIP
26
f_{LO}

FIG. 12

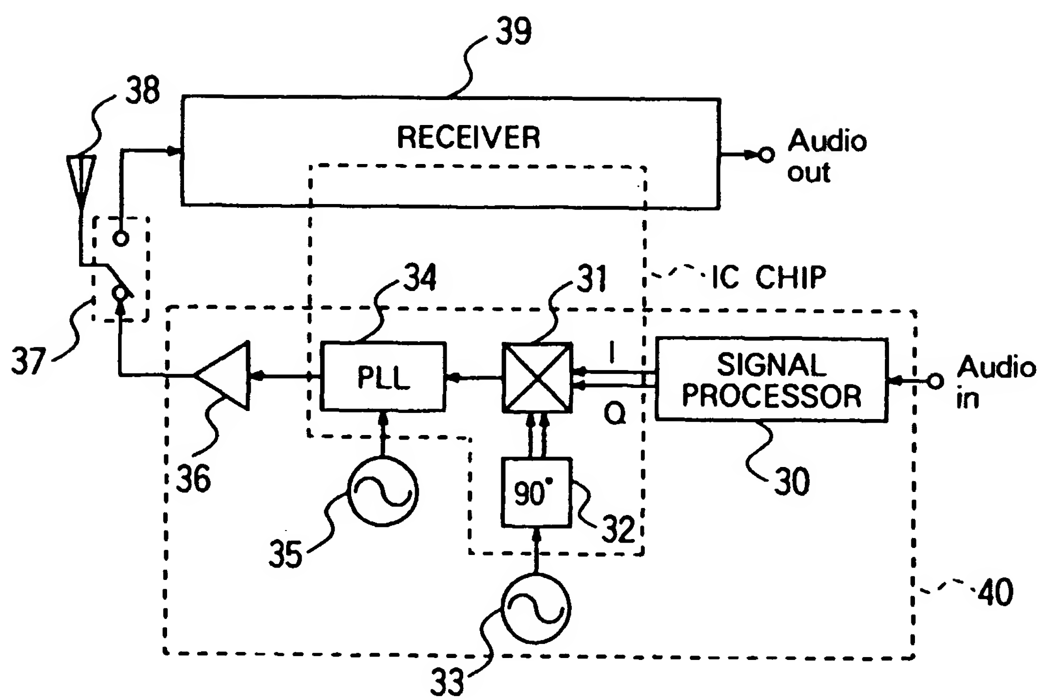

39
38
RECEIVER
Audio out
IC CHIP
34
31
37
PLL
I
SIGNAL PROCESSOR
Audio in
Q
36
30
90°
32
35
40
33

FIG. 13

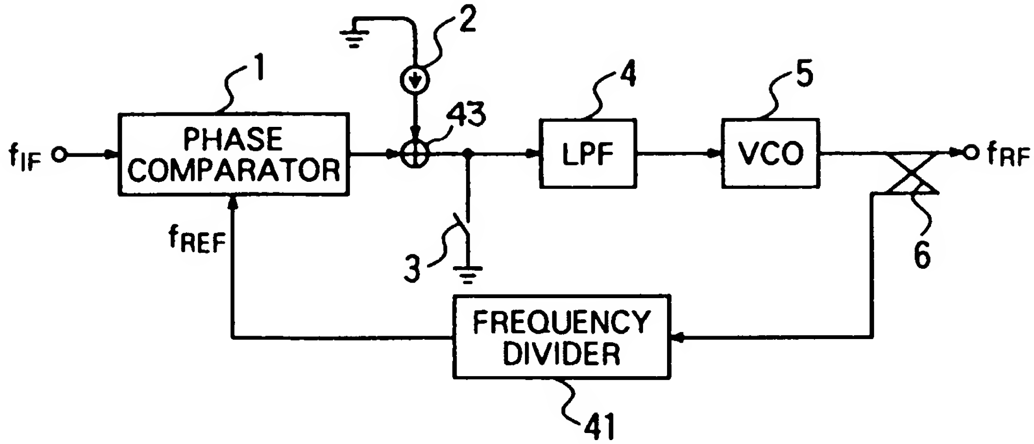
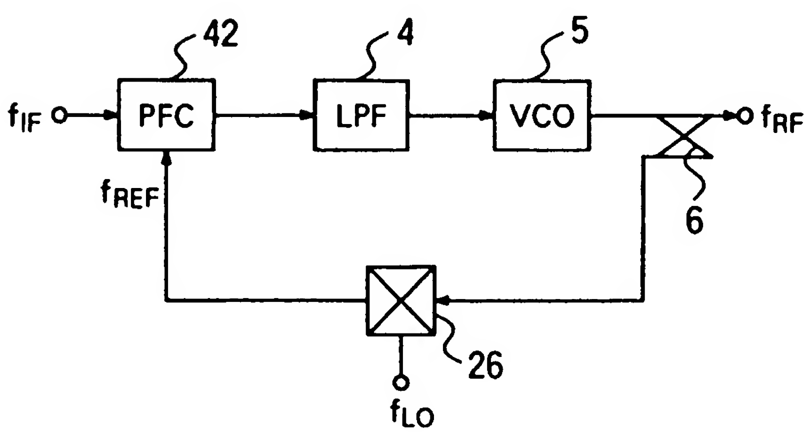

2
1
4
5
43
f_{IF}
PHASE COMPARATOR
LPF
VCO
f_{RF}
f_{REF}
3
6
FREQUENCY DIVIDER
41

FIG. 14


42
4
5
f_{IF}
PFC
LPF
VCO
f_{RF}
f_{REF}
6
26
f_{LO}